IN THE CLAIMS

1. (Original): A method of reducing the pattern effect in the CMP process, comprising the steps of:

(a) providing a semiconductor substrate having a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

(b) performing a first CMP process to remove part of the conductive layer before the barrier layer is polished, thereby a step height of the conductive layer is reduced;

(c) depositing a layer of material substantially the same as the conductive layer over the conductive layer; and

(d) performing a second CMP process to expose the patterned dielectric layer.

2. (Original): The method as claimed in claim 1, wherein the conductive layer comprises copper or copper alloy.

3. (Original):The method as claimed in claim 1, wherein the patterned dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass.

4. (Original): The method as claimed in claim 1, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

5. (Original): The method as claimed in claim 2, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

6. (Original): The method as claimed in claim 1, wherein the top surface of the remaining conductive layer after performing the first CMP process is higher than the barrier layer by more than 10Å.

7.(Original): The method as claimed in claim 6, wherein the top surface of the remaining conductive layer after performing the first CMP process is higher than the barrier layer by from 100Å to 1000Å.

8. (Original): The method as claimed in claim 1, wherein the top surface of the remaining conductive layer after performing the first CMP process is approximately planar.

9. (Original): A method of eliminating dishing phenomena after a CMP process, comprising the steps of:

providing a semiconductor substrate having a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

performing a first CMP process to an end point of polishing to remove part of the conductive layer, wherein the dishing phenomena occur on the conductive layer;

depositing a layer of material substantially the same as the conductive layer over the conductive layer; and

performing a second CMP process to expose the patterned dielectric layer.

10. (Original): The method as claimed in claim 9, wherein the conductive layer comprises copper or copper alloy.

11. (Original): The method as claimed in claim 9, wherein the dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass.

12. (Original): The method as claimed in claim 9, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

13. (Original): The method as claimed in claim 10, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

14. (Original): The method as claimed in claim 9, wherein the top surface of the layer deposited in the step of depositing a layer of material substantially the same as the conductive layer over the conductive layer is higher than the barrier layer.

15. (Currently Amended): A CMP rework method, comprising the steps of:

providing a semiconductor substrate which ~~is reported by a CMP machine as an abnormally polished wafer at a predetermined CMP end point and~~ has a patterned dielectric layer, a barrier layer over the patterned dielectric layer, and a conductive layer over the barrier layer;

performing a first CMP process to remove part of the conductive layer;

depositing a layer of material substantially the same as the conductive layer over the conductive layer; and

performing a second CMP process to expose the patterned dielectric layer.

16. (Original): The method as claimed in claim 15, wherein the conductive layer comprises copper or copper alloy.

17. (Original): The method as claimed in claim 15, wherein the dielectric layer comprises silicon dioxide, silicon nitride, phosphosilicate glass, borophosphosilicate glass, or fluorosilicate glass.

18. (Original): The method as claimed in claim 15, wherein the barrier layer comprises Ta, Ti, TaN, TiN, or WN.

19. (Original): The method as claimed in claim 16, wherein the deposition of copper or copper alloy is performed using electroplating, CVD, or PVD.

20. (Original): The method as claimed in claim 15, wherein the top surface of the layer deposited in the step of depositing a layer of material substantially the same as the conductive layer over the conductive layer is higher than the barrier layer.

21. (New) The method as claimed in claim 15, wherein the semiconductor substrate is reported by a CMP machine as an abnormally polished wafer at a predetermined CMP end point after performing a first CMP process to remove part of the conductive layer.